

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

CERTIFICATE OF MAILING BY "EXPRESS MAIL"

In re Patent Application of:  
**BEAUJOIN ET AL.**

Serial No. **NOT YET ASSIGNED**

Filing Date: **HEREWITH**

For: **A METHOD OF TESTING A SEQUENTIAL  
ACCESS MEMORY PLANE AND A  
CORRESPONDING SEQUENTIAL ACCESS  
MEMORY SEMICONDUCTOR DEVICE**

"EXPRESS MAIL" MAILING LABEL NUMBER **EL 768537528 us**

DATE OF DEPOSIT **FEB. 13, 2002**

I HEREBY CERTIFY THAT THIS PAPER OR FEE IS BEING DEPOSITED  
WITH THE UNITED STATES PATENT AND TRADEMARK OFFICE MAIL POST  
OFFICE IN ORDER TO OBTAIN SERVICE UNDER SECTION 371 OF THE PATENT  
LAW, AND TO BE RECEIVED BY THE COMMISSIONER OF  
PATENTS AND TRADEMARKS, WASHINGTON, D.C. 20501

**Dawn Kimler**  
(TYPED OR PRINTED NAME OF PERSON MAILING PAPER OR FEE)

**Dawn Kimler**  
(SIGNATURE OF PERSON MAILING PAPER OR FEE)

**PRELIMINARY AMENDMENT**

Director, U.S. Patent and Trademark Office  
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of  
the present application, please enter the amendments and  
remarks set out below.

**In the Claims:**

Please cancel Claims 1 to 8.

Please add new Claims 9 to 31.

9. A method of testing a sequential access memory  
array for storing p words each of n bits, the method  
comprising:

writing p test words each made up of n test bits in  
the memory array;

sequentially extracting the p test words from the  
memory array; and

comparing the test bits of the extracted test words  
with expected data bits so that for each test word extracted,  
the corresponding n test bits are compared sequentially with n

2005 FEB 13 10 15 AM '02

In Re Patent Application of  
**BEAUJOIN ET AL.**  
Serial No: **Not Yet Assigned**  
Filing Date: **Herewith**

---

respective expected data bits before extracting the next test word.

10. A method according to Claim 9, wherein the p test words each of n bits are written in such a way as to obtain a checkerboard test binary configuration in the memory array; and further comprising sequentially obtaining the expected data bits by respectively logically combining read addresses of the test words and ranks of the test bits of each test word that is read.

11. A method of testing a sequential access memory array, the method comprising:

writing test words each made up of a plurality of test bits in the memory array;

sequentially extracting the test words from the memory array; and

comparing the test bits of the extracted test words with expected data bits so that for each test word extracted, the corresponding test bits are compared sequentially with respective expected data bits before extracting the next test word.

12. A method according to Claim 11, wherein writing test words in the memory array comprises forming a checkerboard test binary configuration in the memory array.

13. A method according to Claim 12, further comprising sequentially obtaining the expected data bits by respectively logically combining read addresses of the test

In Re Patent Application of  
**BEAUJOIN ET AL.**  
Serial No: **Not Yet Assigned**  
Filing Date: **Herewith**

---

words and ranks of the test bits of each test word that is read.

14. A sequential access semiconductor memory device comprising:

a memory array for storing p words each of n bits;

and

test logic connected to n outputs of the memory array and including

first test means for writing p test words each having n test bits in the array, and

second test means for sequentially extracting the p test words from the memory array and, for each extracted test word, sequentially comparing the corresponding n test bits with n expected data bits, before extracting the next test word.

15. The device according to Claim 14, wherein the second test means comprises:

a set of n connected output registers connected to n respective outputs of the memory array;

first control means for delivering a first control signal to the output registers to simultaneously store the n test bits of a current test word in the output registers;

second control means for delivering a second control signal to the output registers to sequentially shift the test bit contained in each connected output register toward the next connected output register and to sequentially extract the n test bits of the current test word from a last connected output register of the set; and

In Re Patent Application of  
**BEAUJOIN ET AL.**  
Serial No: **Not Yet Assigned**  
Filing Date: **Herewith**

---

comparator means for comparing each bit extracted from the last connected output register with the corresponding expected data bit.

16. The device according to Claim 15, wherein each output register comprises a D-type flip-flop having a data input connected to one of the n outputs of the memory array, a test input, a test output and a test control input for receiving successively and alternately the first control signal and the second control signal; the test output of each flip-flop being connected to the test input of an adjacent flip-flop, the test input of a first flip-flop of the set being receiving an initial data bit, and the test output of the last flip-flop of the set being connected to a first input of the comparator means.

17. The device according to Claim 16, wherein the comparator means comprises one of an EXCLUSIVE OR and EXCLUSIVE NOR logic gate.

18. The device according to Claim 14, wherein the first test means writes the p test words each of n bits to obtain a checkerboard test binary configuration in the memory array; and the test logic further includes generator means for sequentially generating the expected data bits from respective logical combinations of read addresses of the test words and ranks of the test bits of each test word that is read.

19. The device according to Claim 18, wherein the generator means comprises:

In Re Patent Application of  
**BEAUJOIN ET AL.**  
Serial No: **Not Yet Assigned**  
Filing Date: **Herewith**

---

first delivery means for generating a least significant bit of each read address;

a counter for storing a binary word representative of the rank of a test bit in the current test word extracted from the memory array;

second delivery means for generating a least significant bit of each binary word in the counter; and

one of an EXCLUSIVE OR and EXCLUSIVE NOR logic gate comprising two inputs connected to respective outputs of the first and second delivery means, and an output sequentially delivering the expected data bits.

20. A sequential access semiconductor memory device comprising:

a memory array; and

test logic connected to the memory array and

including

a first test circuit for writing test words each having a plurality of test bits in the array, and

a second test circuit for sequentially extracting the test words from the memory array and, for each extracted test word, sequentially comparing the corresponding test bits with expected data bits, before extracting the next test word.

21. The device according to Claim 20, wherein the second test circuit comprises:

a set of connected output registers connected to respective outputs of the memory array;

In Re Patent Application of  
**BEAUJOIN ET AL.**  
Serial No: **Not Yet Assigned**  
Filing Date: **Herewith**

---

a first control device for delivering a first control signal to the output registers to simultaneously store the test bits of a current test word in the output registers;

a second control device for delivering a second control signal to the output registers to sequentially shift the test bit contained in each connected output register toward the next connected output register and to sequentially extract the test bits of the current test word from a last connected output register of the set; and

a comparator for comparing each bit extracted from the last connected output register with the corresponding expected data bit.

22. The device according to Claim 21, wherein each output register comprises a D-type flip-flop having a data input connected to one of the outputs of the memory array, a test input, a test output and a test control input for receiving successively and alternately the first control signal and the second control signal; the test output of the flip-flops being connected to the test input of an adjacent flip-flop, the test input of a first flip-flop of the set receiving an initial data bit, and the test output of the last flip-flop of the set being connected to a first input of the comparator.

23. The device according to Claim 22, wherein the comparator comprises one of an EXCLUSIVE OR and EXCLUSIVE NOR logic gate.

In Re Patent Application of  
**BEAUJOIN ET AL.**  
Serial No: **Not Yet Assigned**  
Filing Date: **Herewith**

---

24. The device according to Claim 20, wherein the first test circuit writes the p test words each of n bits to obtain a checkerboard test binary configuration in the memory array; and the test logic further includes an expected bit generator for sequentially generating the expected data bits from respective logical combinations of read addresses of the test words and ranks of the test bits of each test word that is read.

25. The device according to Claim 24, wherein the generator comprises:

a first bit generator for generating a least significant bit of each read address;

a counter for storing a binary word representative of the rank of a test bit in the current test word extracted from the memory array;

a second bit generator for generating a least significant bit of each binary word in the counter; and

a logic gate comprising two inputs connected to respective outputs of the first and second delivery circuits, and an output sequentially delivering the expected data bits.

26. A test circuit for a sequential access semiconductor memory device having a memory array, the test circuit comprising:

a first test circuit for writing test words each having a plurality of test bits in the array; and

a second test circuit for sequentially extracting the test words from the memory array and, for each extracted

In Re Patent Application of  
**BEAUJOIN ET AL.**  
Serial No: **Not Yet Assigned**  
Filing Date: **Herewith**

---

test word, sequentially comparing the corresponding test bits with expected data bits, before extracting the next test word.

27. The circuit according to Claim 26, wherein the second test circuit comprises:

a set of connected output registers connected to respective outputs of the memory array;

a first control device for delivering a first control signal to the output registers to simultaneously store the test bits of a current test word in the output registers;

a second control device for delivering a second control signal to the output registers to sequentially shift the test bit contained in each connected output register toward the next connected output register and to sequentially extract the test bits of the current test word from a last connected output register of the set; and

a comparator for comparing each bit extracted from the last connected output register with the corresponding expected data bit.

28. The circuit according to Claim 27, wherein each output register comprises a D-type flip-flop having a data input connected to one of the outputs of the memory array, a test input, a test output and a test control input for receiving successively and alternately the first control signal and the second control signal; the test output of the flip-flops being connected to the test input of an adjacent flip-flop, the test input of a first flip-flop of the set receiving an initial data bit, and the test output of the last



In Re Patent Application of  
**BEAUJOIN ET AL.**  
Serial No: **Not Yet Assigned**  
Filing Date: **Herewith**

---

flip-flop of the set being connected to a first input of the comparator.

29. The circuit according to Claim 28, wherein the comparator comprises one of an EXCLUSIVE OR and EXCLUSIVE NOR logic gate.

30. The circuit according to Claim 26, wherein the first test circuit writes the p test words each of n bits to obtain a checkerboard test binary configuration in the memory array; and the test logic further includes an expected bit generator for sequentially generating the expected data bits from respective logical combinations of read addresses of the test words and ranks of the test bits of each test word that is read.

31. The circuit according to Claim 30, wherein the generator comprises:

a first bit generator for generating a least significant bit of each read address;

a counter for storing a binary word representative of the rank of a test bit in the current test word extracted from the memory array;

a second bit generator for generating a least significant bit of each binary word in the counter; and

a logic gate comprising two inputs connected to respective outputs of the first and second delivery circuits, and an output sequentially delivering the expected data bits.

In Re Patent Application of  
**BEAUJOIN ET AL.**  
Serial No: **Not Yet Assigned**  
Filing Date: **Herewith**


---

**REMARKS**

For better readability and the Examiner's convenience, the newly submitted claims differ from the translated foreign counterpart claims which are being canceled. The newly submitted claims do not represent changes or amendments that narrow the claim scope for any reason related to the statutory requirements for patentability.

It is believed that all of the claims are patentable over the prior art. Accordingly, after the Examiner completes a thorough examination, a Notice of Allowance is respectfully requested in due course. If any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number below.

Respectfully submitted,



---

PAUL J. DITMYER  
Reg. No. 40,455  
Allen, Dyer, Doppelt, Milbrath  
& Gilchrist, P.A.  
255 S. Orange Avenue, Suite 1401  
Post Office Box 3791  
Orlando, Florida 32802  
407-841-2330  
407-841-2343 fax  
Attorneys for Applicants